EXP 1

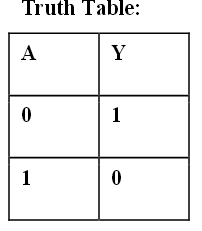
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M.S.SANJAY

**NOT gate**

NOT

A NOT gate is made by joining the inputs of a NAND gate. Since a NAND gate is equivalent to an AND gate followed by a NOT gate, joining the inputs of a NAND gate leaves only the NOT part.

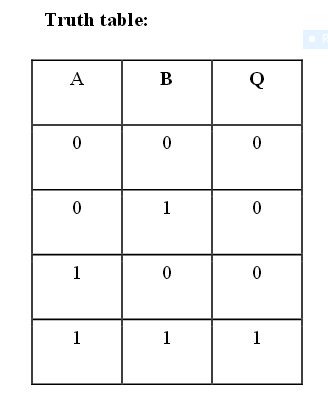


**AND GATE**

AND

An AND gate is made by following a NAND gate with a NOT gate as

shown below. This gives a NOT NAND, i.e. AND

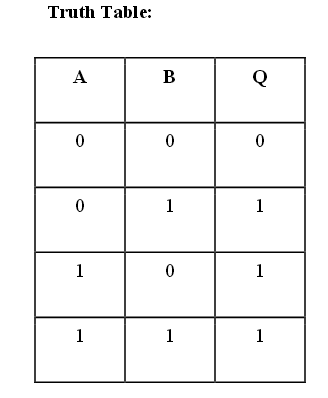


**OR Gate**

OR

If the truth table for a NAND gate is examined or by applying De Morgan's Laws, it can be seen that if any of the inputs are 0, then the output will be 1. However to be an OR gate, if any input is 1, the

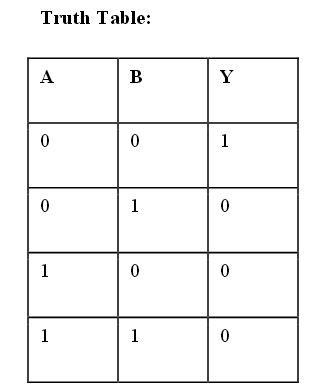
output must also be 1. Therefore, if the inputs are inverted, any high input will trigger a high output.



NOR Gate

NOR

A NOR gate is simply an OR gate with an inverted output



**XOR Gate**

XOR

An XOR gate is constructed similarly to an OR gate, except with an additional NAND gate inserted such that if both inputs are high, the inputs to the final NAND gate will also be high, and the output will be low. This effectively represents the formula: "NAND(A NAND (A NAND B)) NAND (B NAND (A NAND B))".

